

# PHP/PHB/PHD66NQ03LT

TrenchMOS™ logic level FET

Rev. 04 — 9 September 2002

Product data

## 1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP66NQ03LT in SOT78 (TO-220AB)

PHB66NQ03LT in SOT404 (D<sup>2</sup>-PAK)

PHD66NQ03LT in SOT428 (D-PAK).

## 2. Features

- Low on-state resistance
- Fast switching.

## 3. Applications

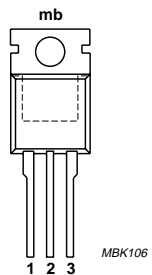
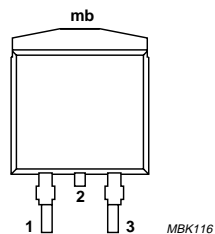
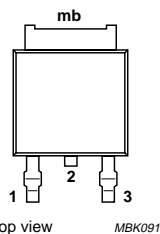
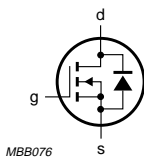
- High frequency computer motherboard DC to DC converters.

## 4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		

			
<b>SOT78 (TO-220AB)</b>	<b>SOT404 (D<sup>2</sup>-PAK)</b>	<b>SOT428 (D-PAK)</b>	

[1] It is not possible to make connection to pin 2 of the SOT404 and SOT428 packages.

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	66	A
		$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	57	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	93	W
$T_j$	junction temperature		-	175	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	9.1	12	mΩ
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	12.3	16	mΩ

## 6. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

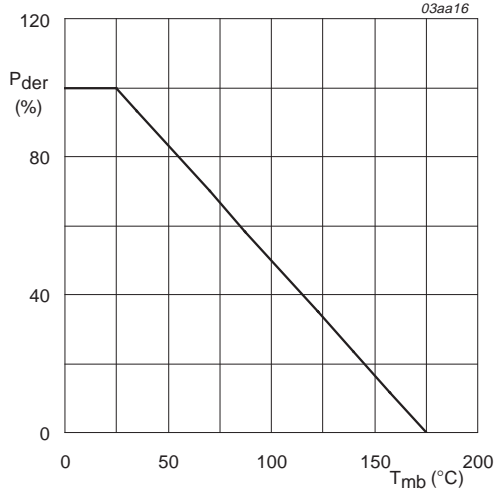
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	25	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2 and 3</b>	-	57	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2</b>	-	40	A
		$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$	-	66	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}$	-	45	A
$V_{GS}$	gate-source voltage		-	±20	V
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	-	228	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <b>Figure 1</b>	-	93	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C

### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	57	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	228	A

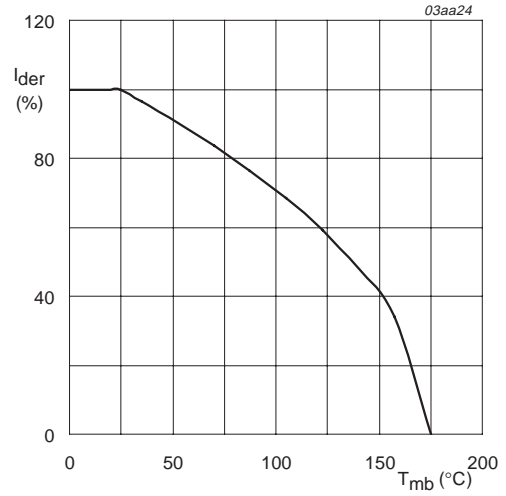
### Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A};$ $t_p = 0.15\text{ ms}; V_{DD} \leq 15\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V};$ starting $T_j = 25\text{ °C}$	-	90	mJ
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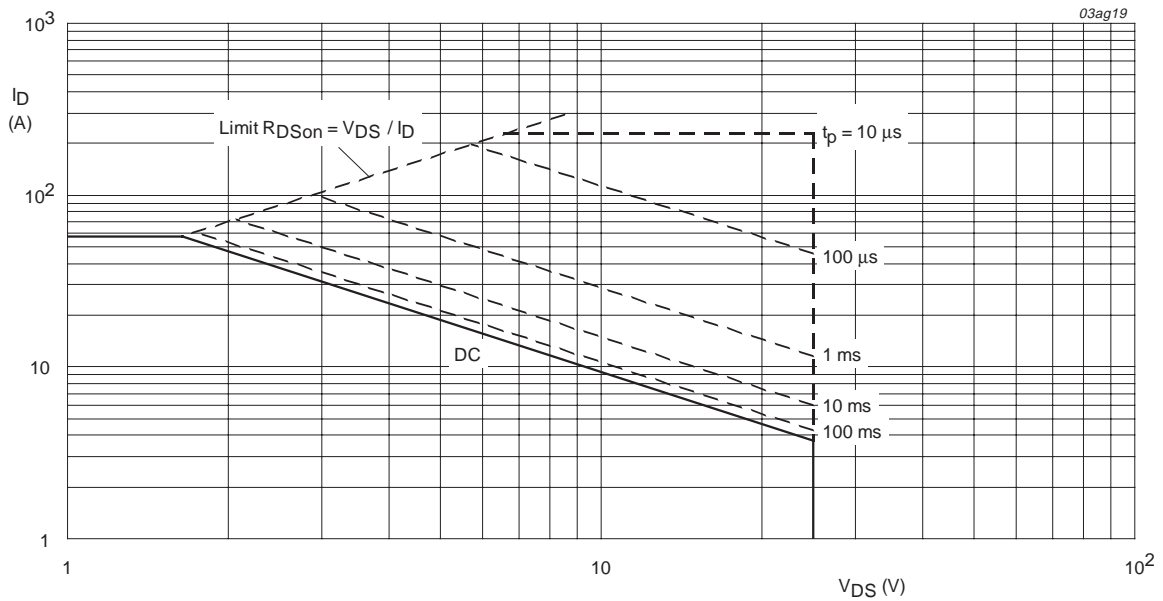
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 5 V$ .

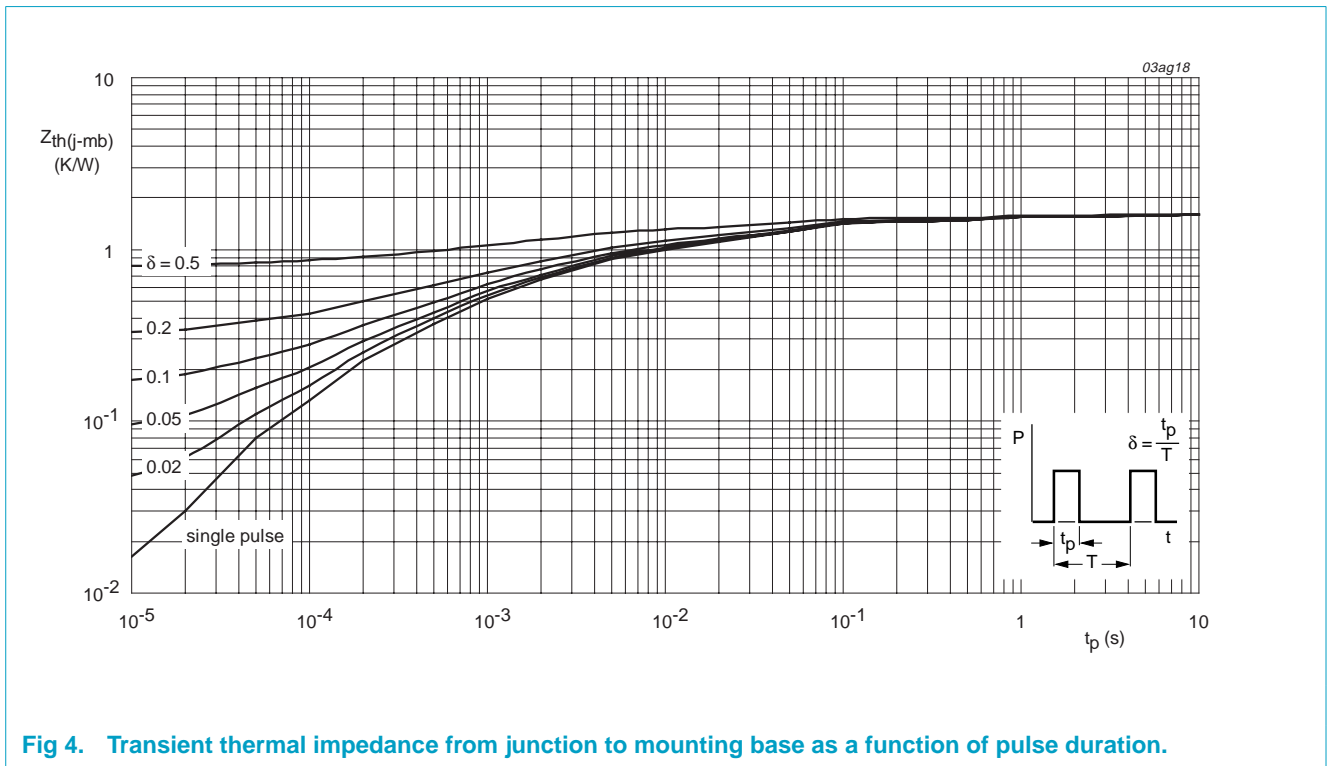
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT428	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
	SOT404 and SOT428	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

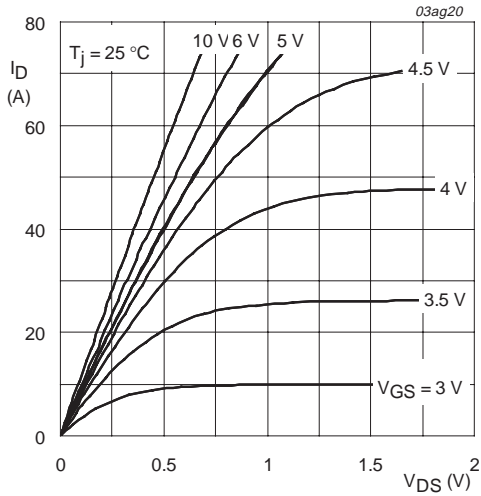
### 7.1 Transient thermal impedance



## 8. Characteristics

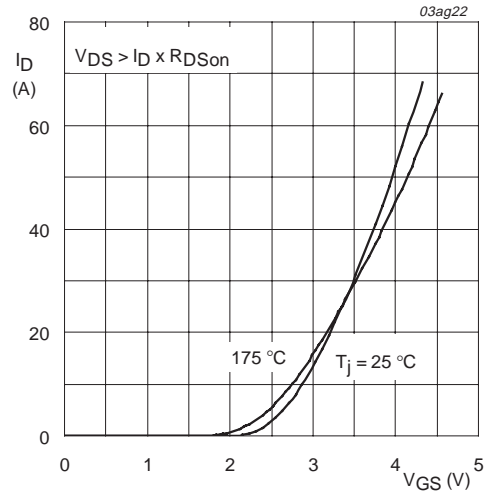
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	25	-	-	V
		T <sub>j</sub> = -55 °C	22	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <b>Figure 9</b>				
		T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 175 °C	0.5	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.3	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	10	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±5 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; <b>Figure 7 and 8</b>				
		T <sub>j</sub> = 25 °C	-	12.3	16	mΩ
		T <sub>j</sub> = 175 °C	-	22.1	28.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A				
		T <sub>j</sub> = 25 °C	-	9.1	12	mΩ
<b>Dynamic characteristics</b>						
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 30 A	-	40	-	S
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 50 A; V <sub>DD</sub> = 15 V; V <sub>GS</sub> = 5 V; <b>Figure 13</b>	-	12	-	nC
Q <sub>gs</sub>	gate-source charge		-	4.5	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	3.6	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; <b>Figure 11</b>	-	860	-	pF
C <sub>oss</sub>	output capacitance		-	330	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	145	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 15 V; I <sub>D</sub> = 25 A; V <sub>GS</sub> = 5 V;	-	15	25	ns
t <sub>r</sub>	rise time	R <sub>G</sub> = 5.6 Ω; resistive load	-	90	135	ns
t <sub>d(off)</sub>	turn-off delay time		-	25	40	ns
t <sub>f</sub>	fall time		-	25	40	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.95	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	32	-	ns
Q <sub>r</sub>	recovered charge		-	20	-	nC



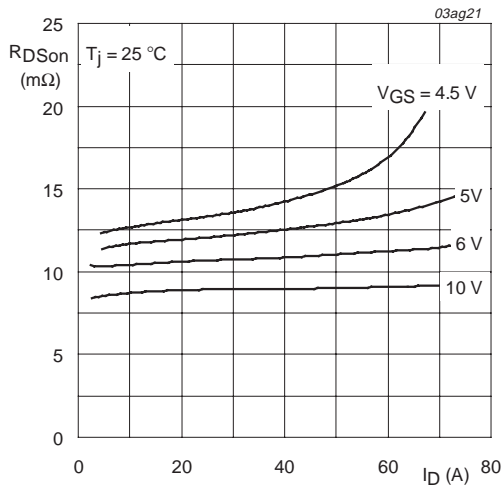
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



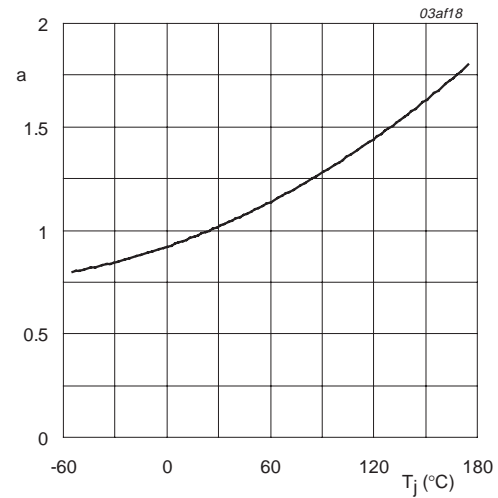
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



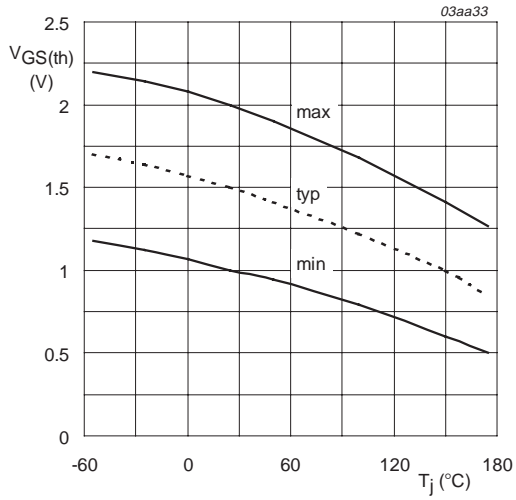
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



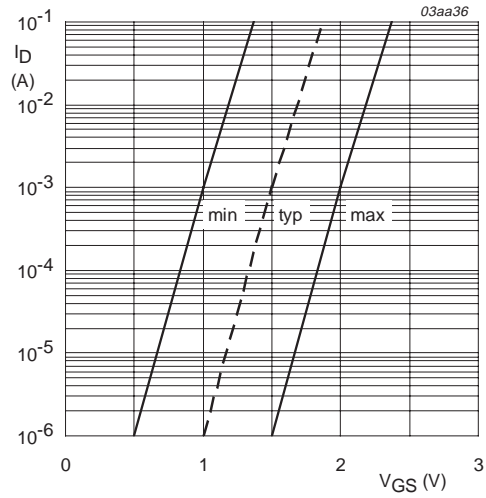
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



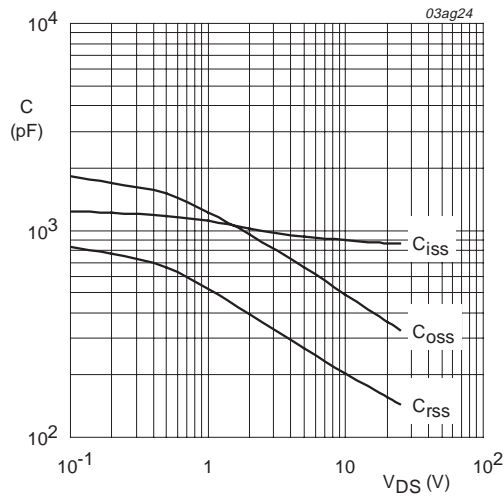
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



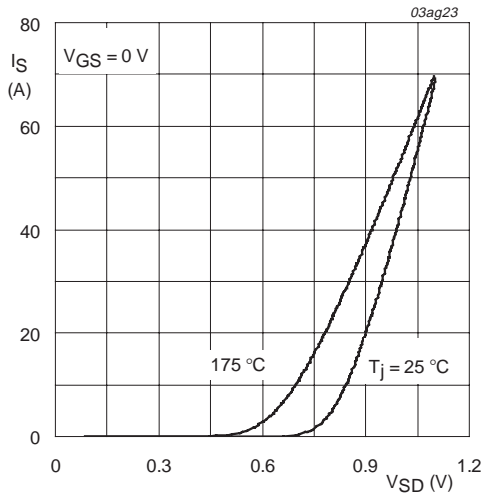
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



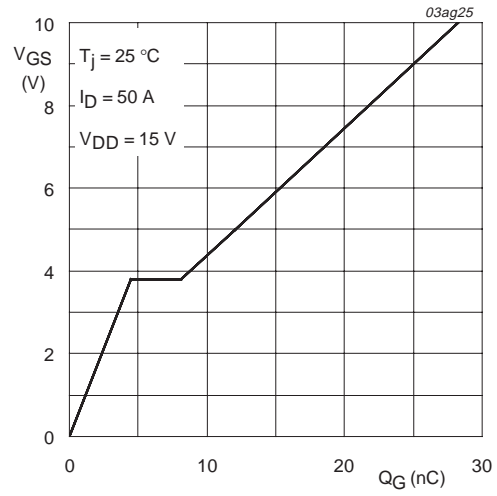
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25\text{ °C}$  and  $175\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 50\text{ A}$ ;  $V_{DD} = 15\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

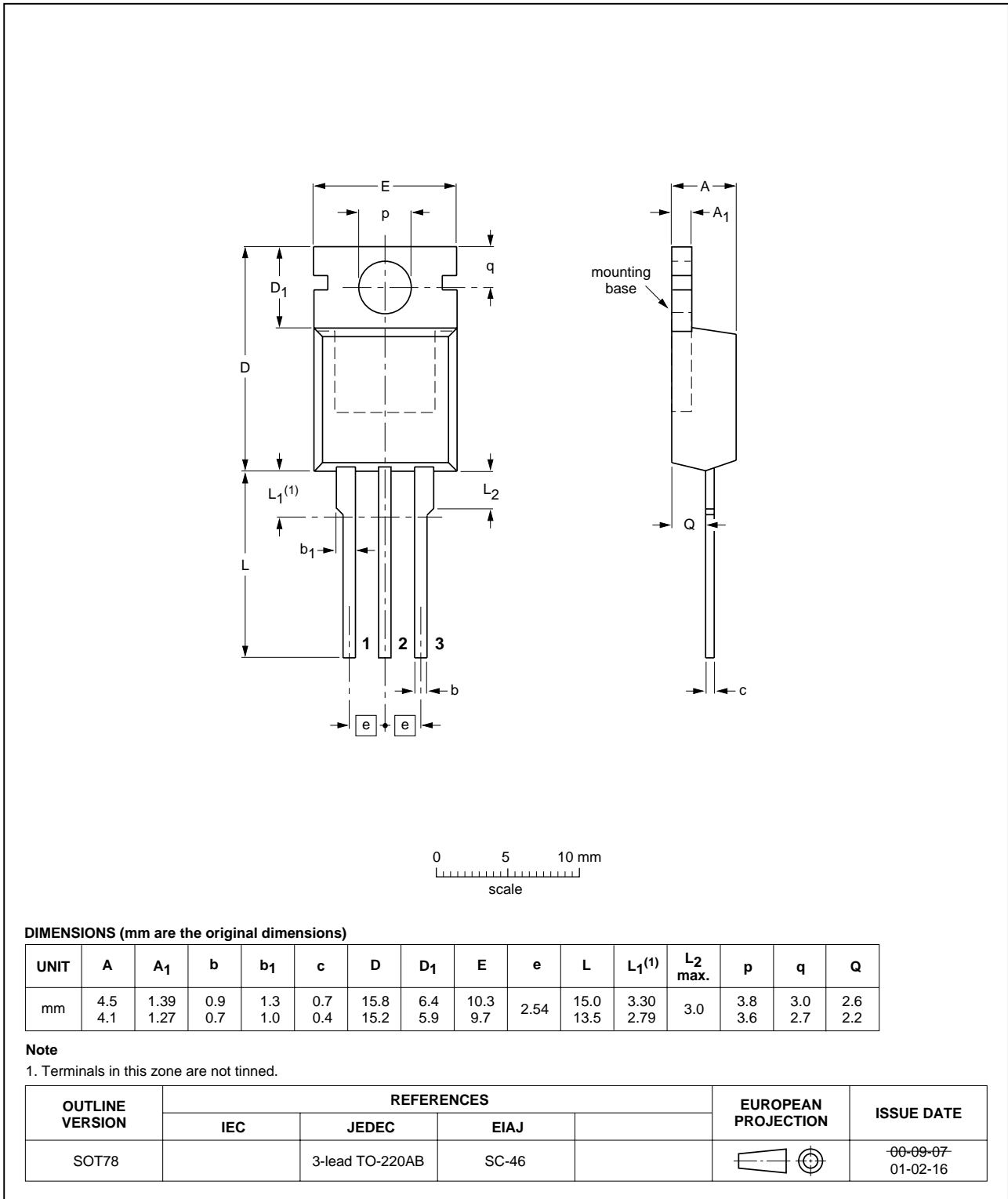


Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

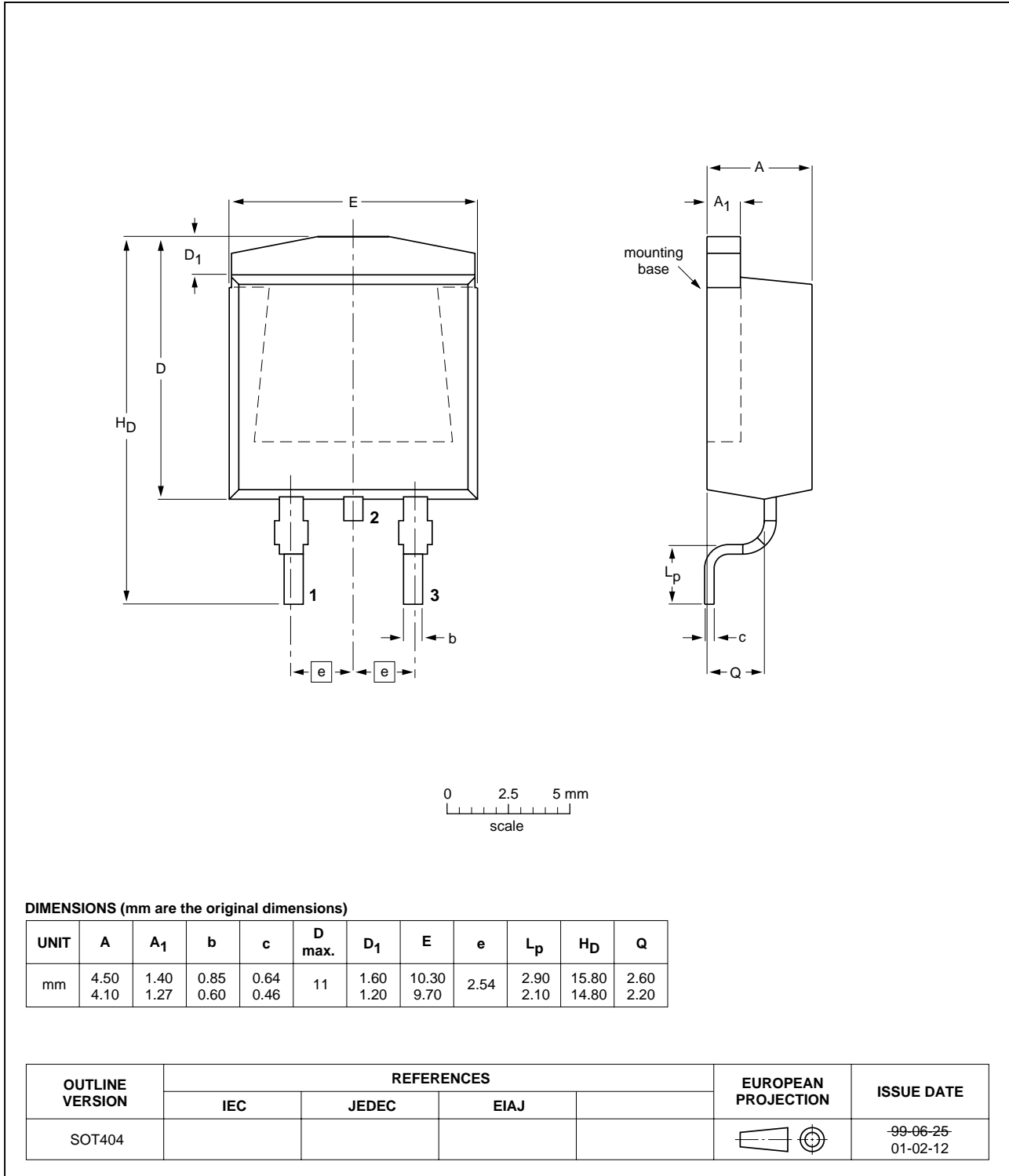


Fig 15. SOT404 (D<sup>2</sup>-PAK).

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads  
(one lead cropped)

SOT428

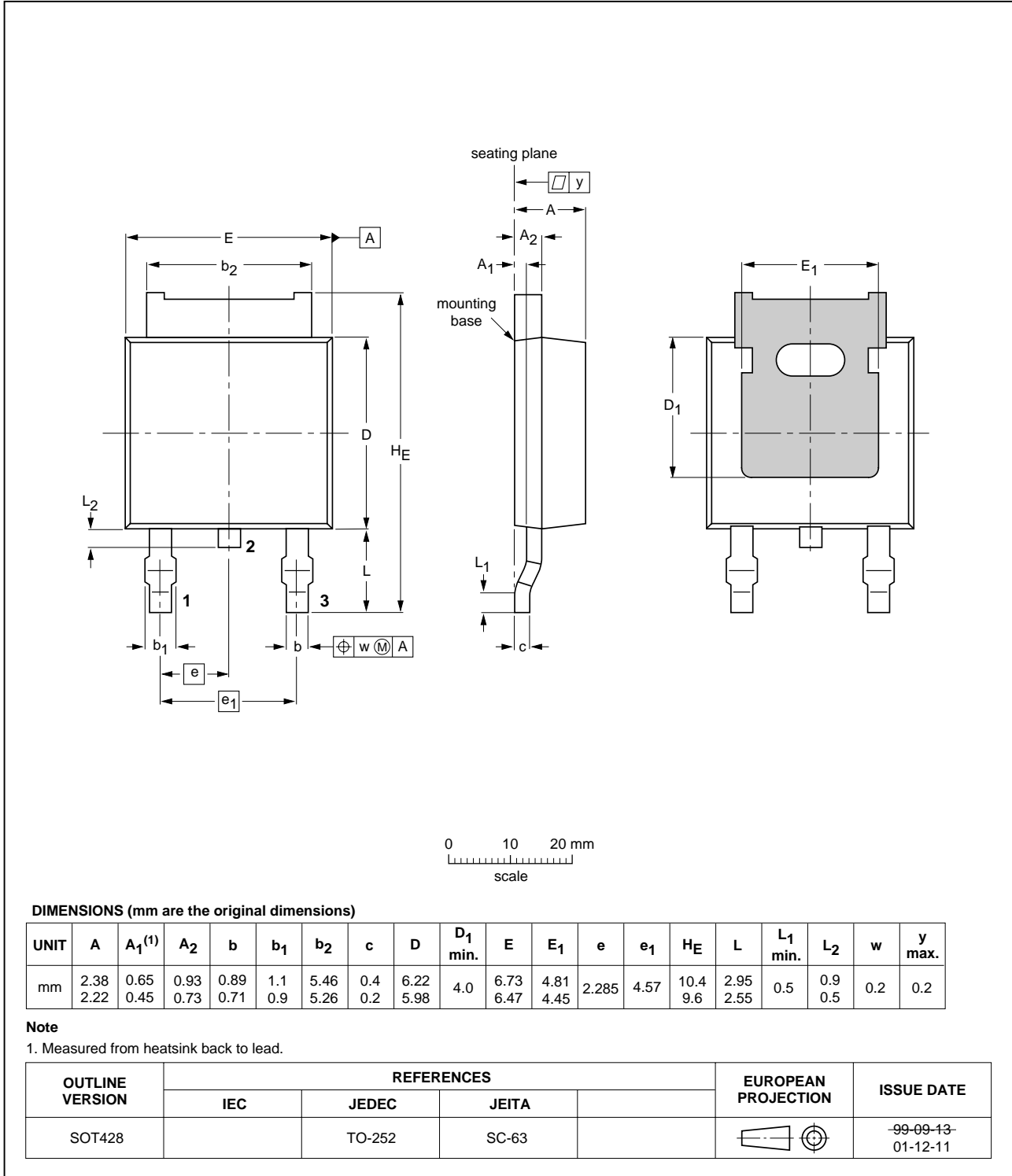


Fig 16. SOT428 (D-PAK)

## 10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
04	20020909	-	<b>Product data; fourth version; supersedes version of 12 March 2002.</b> <b>Section 6 "Limiting values"</b> Addition of $E_{DS(AL)S}$ . Graphs updated to latest standard.
03	20020312	-	<b>Product data; third version; supersedes version of 10 December 2001.</b> <b>Section 6 "Limiting values"</b> Standardized $V_{GS}$ rating. <b>Section 7 "Thermal characteristics"</b> Clarification of thermal resistances table. <b>Section 8 "Characteristics"</b> Improved Gate charge and Capacitance.
02	20011210	-	<b>Includes product data; second version; supersedes initial version 12 October 2001.</b> • <b>Section 1 "Description"</b> Correction to typing mistake in name.
01	20011012	-	<b>Product data; initial version</b>

## 11. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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